IN THE CLAIMS:

Claims 61 and 66 have been amended herein. Please note that all claims currently pending and under consideration in the referenced application are shown below. Please enter these claims as amended. This listing of claims will replace all prior versions and listings of claims in the application.

~~Listing of Claims:~~

1-60. (canceled)

61. (currently amended) A process for fabricating a capacitor on a substrate, said process comprising the steps of:

providing a first insulating layer on said substrate, said first insulating layer having an opening therein forming a container;

forming a generally conformal first conductive layer, having a second etch rate, over said first insulating layer and in said container;

forming a second insulating layer above said first conductive layer; and

removing at least a portion of said second insulating layer through use of chemical mechanical planarization until an upper portion of said first conductive layer is exposed.

62. (original) The process of claim 61, further comprising the step of removing at least a portion of said upper portion of said first conductive layer until said first insulating layer is exposed.

63. (original) The process of claim 61, wherein said second insulating layer is a sacrificial layer conducive to said chemical mechanical planarization.

64. (original) The process of claim 61, wherein said first and said second insulating layers are oxides.

65. (original) The method of claim 61, wherein said first insulating layer is subject to a first etch rate and said second insulating layer is subject to a second etch rate, and wherein said first etch rate is a lower etch rate than said second etch rate.

66. (currently amended) A process for fabricating a DRAM containing storage capacitor on a silicon substrate having an existing topography including active areas, word lines and digit lines, said process comprising the steps of:

providing a first insulating layer having a first etch rate, over said existing topography;

forming an opening into said first insulating layer, said opening thereby forming a container;

forming a conformal first conductive layer over said first insulating layer and said container, thereby lining said container;

forming a second insulating layer, having a second etch rate, over said first conductive layer; and

removing said second insulating layer through use of chemical mechanical planarization until an upper portion of said first conductive layer is exposed.

67. (original) The process of claim 66, further comprising the step of removing at least a portion of said upper portion of said first conductive layer until said first insulating layer is exposed, thereby forming a conductive container having inner and outer walls.

68. (original) The process of claim 66, wherein said second insulating layer is a sacrificial layer conducive to said chemical mechanical planarization.

69. (original) The process of claim 66, wherein said first and said second insulating layers are oxides.

70. (original) The method of claim 66, wherein said first insulating layer etch rate is a lower etch rate than said second insulating layer etch rate.

71. (original) A process for fabricating a DRAM container storage capacitor on a silicon substrate having an existing topography including active areas, word lines and digit lines, said process comprising the steps of:

providing a first insulating layer, having a first etch rate, over said existing topography;

forming an opening into said first insulating layer, said opening thereby forming a container;

forming a conformal first conductive layer over said first insulating layer and said container, thereby lining said container;

forming a second insulating layer, having a second etch rate, over said first conductive layer; and

removing said second insulating layer through use of chemical mechanical planarization until an upper portion of said first conductive layer is exposed;

removing at least a portion of said upper portion of said first conductive layer until said first insulating layer is exposed, thereby forming a conductive container having inner and outer walls.